WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit that is connected to an external load and a power supply, comprising:

a lead frame;

a first lead wire connected to a high electric potential side of the power supply;

a second lead wire connected to a high electric potential side of the external load;

a third lead wire connected to a low electric potential side of the external load;

a transistor that is one of a P-channel type and a PNP type, the P-channel type having a source connected to the first lead wire and having a drain connected to the second lead wire, and the PNP type having an emitter connected to the first lead wire and having a collector connected to the second lead wire; and

a diode for circulating an electrical current and having a cathode and an anode, the cathode being connected to the second lead wire, and the anode being connected to the third lead wire,

wherein the transistor and the diode are mounted on a single island of the lead frame.

2. The semiconductor integrated circuit according to claim 1, further comprising:

a resin member that covers the transistor, the diode, and the lead frame, and exposes a non-chip-mounted surface of

the island.

3. The semiconductor integrated circuit according to claim 2, wherein the island is depressed so that the non-chip-mounted surface of the depressed island is exposed from the resin member.

4. The semiconductor integrated circuit according to claim 2, wherein the island has a thick portion on which the diode and the transistor are mounted so that the non-chip-mounted surface of the thick portion of the island is exposed from the resin member.

5. The semiconductor integrated circuit according to claim 1, further comprising:

a plate member having high thermal conductivity and integrally mounted to the island on which the transistor and the diode are mounted; and

a resin member that covers the transistor, the diode, the lead frame, and the plate member, and exposes a non-chip-mounted surface of the plate member.

6. The semiconductor integrated circuit according to claim 2, further comprising:

a cooling plate mounted to the exposed surface of the island.

7. The semiconductor integrated circuit according to claim 2, wherein the non-chip-mounted surface of the island is flush with a surface of the resin member.

8. The semiconductor integrated circuit according to claim 1, wherein the cathode of the diode and one of the drain of the P-channel transistor and the collector of the PNP transistor are connected to the island.

9. A semiconductor integrated circuit having a lead frame, comprising:

a transistor that has a first terminal connected to a first lead wire and a second terminal connected to a second lead wire; and

a diode having a cathode and an anode, the cathode being connected to the second lead wire, and the anode being connected to a third lead wire,

wherein the second terminal of the transistor and the cathode of the diode have a common electrical potential, and

the transistor and the diode are mounted on a single island of the lead frame so that the second terminal of the transistor and the cathode of the diode are connected to the island.

10. The semiconductor integrated circuit according to claim 9, wherein the transistor is a P-channel type, the first terminal of the transistor is a source of the P-channel

transistor, and the second terminal of the transistor is a drain of the P-channel transistor.

11. The semiconductor integrated circuit according to claim 9, wherein the transistor is a PNP type, the first terminal of the transistor is an emitter of the PNP type, and the second terminal of the transistor is a collector of the PNP type.

12. The semiconductor integrated circuit according to claim 9, wherein the first lead wire is connected to a high electric potential side of a power supply, the second lead wire is connected to a high electric potential side of an external load, and the third lead wire is connected to a low electric potential side of the external load.